REMARKS

This paper is responsive to a Final Office action dated July 28, 2006. Claims 1, 27 and 28 were examined, and were rejected.

Claim Amendments

Withdrawn claims 55-60 have been canceled without prejudice to the subject matter therein.

Claim Rejections under 35 U.S.C. § 102

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,380,636 (hereinafter "Tatsukawa"). Applicant respectfully traverses this rejection.

The Examiner cites Tatsukawa, in Fig. 8, as disclosing a NAND string memory array, each NAND string "including at a first end thereof a respective plurality of series selection devices of like type, wherein each NAND string includes a second plurality of series selection devices of like type at a second end thereof." Relative to the NAND string shown on the left side of Fig. 8, the Examiner cites transistors DG1 and SGD1 as corresponding to the plurality of series selection devices at the first end of the NAND string, and cites transistors SGS1 and DG2 as corresponding to the plurality of series selection devices at the second end of the NAND string.

Applicant agrees with the Examiner's position regarding transistors DG1 and SGD1, but respectfully takes issue with the position regarding transistors SGS1 and DG2. Applicant submits that only transistor SGS1 corresponds to a selection device at this end of this NAND string because the connection to the source line SL1 is made just "beyond" transistor SGS1, as viewed from the perspective of the NAND string. Specifically, the common node between transistors SGS1 and DG2 is itself the source line SL1. Tatsukawa describes the role of transistor DG2 as being for matching purposes in his description regarding Fig. 1 (even though described in the context of a different memory cell arrangement than Fig. 8), to wit:

> These dummy transistors DG1-DG4 are employed so that sub-bit lines SBL1 and SBL2 may have the same electric characteristics (parasitic

> resistance and parasitic capacitances) and sub-source lines SSL1 and SSL2 may have the same electric characteristics. Owing to these dummy transistors DG1-DG4, the layout of transistors in memory cell unit MU can be symmetrical with respect to main bit line MBL, so that the layout can be made simple, and an influence by misalignment of a mask in a manufacturing process can be cancelled. By arranging the source line between the source select signal lines, the size of the unit in the column direction can be reduced.

(Tatsukawa, column 7, lines 50-61). The source (or drain) region of this transistor DG2 is also shown in Fig. 5 as impurity region 2-1a. This appears to be an unconnected impurity region, as the array shown in Fig. 6 does not indicate any nodes leaving a respective memory cell unit MU except the two connections to the main bit line MBL, nor any other connections common to adjacent memory units MU. Nonetheless, it is not clear whether Tatsukawa intends to "abut" the impurity region 2-1a with the impurity region 1-1a within a second memory cell unit MU adjacent to ("below" as drawn) the one shown in Fig. 5 (see column 10, lines 25-26, "These diffusion layers all extend in the column direction."), or alternately, whether Tatsukawa intends to provide space between such adjacent impurity regions.

A resolution to this question is unnecessary because, in either case, dummy transistor DG2 *cannot be seen as a select device.* A select device within, and at one end of, a NAND string functions to couple a series connected string of memory cells within the NAND string to some kind of memory array node (e.g., global array line, main bit line, bias node, source line, etc.). Tatsukawa's dummy transistor DG2 does not couple memory cells within the NAND string (i.e., memory cells MC11, MC12) to the source line SL1, and thus cannot be seen as a select device. Rather, only transistor SGS1 functions to couple the memory cells MC11, MC12 to the source line SL1.

Any extraneous transistor structure formed "beyond" the connection to the memory array node in question is not part of the NAND string. In this case, the extraneous dummy transistor DG2 is connected to the same source line SL1, but is not part of the NAND string, does not function to select the NAND string, and cannot be seen as being a select device.

As used in the instant application, this transistor DG2 cannot be seen as one of a *plurality* of series select transistors *at one end* of the NAND string (i.e., "each NAND string including at a

first end thereof a plurality of series select devices ..."). Consequently this NAND string does not include a plurality of series selection devices at *both ends* of the NAND string.

The similar situation is present for the NAND string shown on the right side of Fig. 8. Applicant submits that transistor DG4 is not part of the NAND string since it lies beyond the connection to node SL2, and consequently the second NAND string likewise does not include a plurality of series selection devices at both of its ends.

Applicant submits that Tatsukawa fails to disclose each limitation of claim 1, and that the Examiner has therefore not established a prima facie case for anticipation. Applicant respectfully requests the rejection be withdrawn.

Claim Rejections under 35 U.S.C. § 103

Claims 27-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Tatsukawa in view of U.S. Patent No. 6,411,548 (hereinafter "Sakui"). These two claims are believed allowable at least for their dependence from allowable claim 1.

Summary

In summary, claims 1-20, 22-23, and 27-54 remain in the case. Claims 1, 27, and 28 remain under examination. Claims 2-20, 22-23, and 29-54 remain withdrawn from consideration.

All pending claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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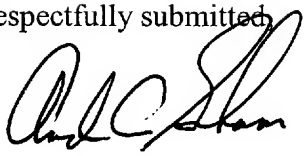
Respectfully submitted,



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